

What is claimed is:

1 1. A collar dielectric process, comprising the steps
2 of:
3 providing a semiconductor silicon substrate having a
4 deep trench and a deep trench capacitor, in which
5 the deep trench capacitor comprises a node
6 dielectric formed on the sidewall and bottom of
7 the deep trench and a storage node formed in the
8 deep trench and reaching a predetermined depth;
9 performing an ion implantation process to form an ion
10 implantation area on the substrate at the top of
11 the deep trench;
12 removing the node dielectric until the top of the node
13 dielectric is leveled off with the top of the
14 storage node, thus exposing the sidewall of the
15 deep trench outside the deep trench capacitor;
16 and
17 performing an oxidation process to grow a first silicon
18 oxide layer on the exposed sidewall of the deep
19 trench, in which the first silicon layer is
20 outside the ion implantation area.

1 2. The collar dielectric process as claimed in claim
2 1, wherein the ion implantation process uses N₂ as the ion
3 source to restrain the growth of the first silicon oxide
4 layer.

1 3. The collar dielectric process as claimed in claim
2 1, wherein the position and vertical length of the ion

Client's ref. : 91146
Our ref: 0548-9814-us/final/Cherry

3 implantation area corresponds to those of a buried strap
4 outdiffusion region.

1 4. The collar dielectric process as claimed in claim
2 1, wherein the ion implantation process partially surrounds
3 a partial top of the deep trench and is adjacent to a buried
4 strap outdiffusion region.

1 5. The collar dielectric process as claimed in claim
2 1, wherein the ion implantation process entirely surrounds
3 the top of the deep trench.

1 6. The collar dielectric process as claimed in claim
2 1, wherein the vertical length of the ion implantation area
3 is 800~1500Å.

1 7. The collar dielectric process as claimed in claim
2 1, wherein the node dielectric is a silicon nitride layer.

1 8. The collar dielectric process as claimed in claim
2 1, wherein the storage node is an n⁺-doped polysilicon
3 layer.

1 9. The collar dielectric process as claimed in claim
2 1, wherein the deep trench capacitor further comprises a
3 buried plate which is an n⁺-type diffusion region formed in
4 the substrate at the lower portion of the deep trench and
5 surrounding the node dielectric.

1 10. The collar dielectric process as claimed in claim
2 1, further comprising the steps of:

3 forming a second silicon oxide layer on the sidewall of
4 the deep trench to cover the first silicon oxide
5 layer and the ion implantation area;
6 forming a first conductive layer in the deep trench to
7 connect the top of the storage node;
8 recessing the first conductive layer until reaching a
9 predetermined depth; and
10 etching the second silicon oxide layer and the first
11 silicon oxide layer to level off the top of the
12 second silicon oxide layer and the top of the
13 first silicon oxide layer until the top of the
14 first conductive layer protrudes from the tops of
15 the second silicon oxide layer and the first
16 silicon oxide layer, wherein the combination of
17 the second silicon oxide layer and the first
18 silicon oxide layer remaining on the sidewall of
19 the deep trench serve as a collar dielectric
20 layer.

1 11. The collar dielectric process as claimed in claim
2 10, wherein the first conductive layer is an n⁺-doped
3 polysilicon layer.

1 12. The collar dielectric process as claimed in claim
2 10, further comprising the steps of:
3 forming a second conductive layer in the deep trench;
4 and
5 forming a buried strap outdiffusion region in the
6 silicon substrate adjacent to the second
7 conductive layer, wherein the position and
8 vertical length of the buried strap outdiffusion

Client's ref. :91146
Our ref: 0548-9814-us/final/Cherry

9 region correspond to those of the ion
10 implantation area.

1 13. The collar dielectric process as claimed in claim
2 12, wherein the second conductive layer is a polysilicon
3 layer.

1 14. The collar dielectric process as claimed in claim
2 12, wherein the buried strap outdiffusion region is an n⁺-
3 type diffusion region.